

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Takashi YAMADA, et al.

GAU:

SERIAL NO: New CONT Application

EXAMINER:

FILED: Herewith

FOR: SEMICONDUCTOR CHIP HAVING MULTIPLE FUNCTIONAL BLOCKS INTEGRATED IN A SINGLE CHIP AND METHOD FOR FABRICATING THE SAME

REQUEST FOR PRIORITY

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

- ☒ Full benefit of the filing date of U.S. Application Serial Number 09/995,594, filed November 29, 2001, is claimed pursuant to the provisions of **35 U.S.C. §120**.
- ☐ Full benefit of the filing date(s) of U.S. Provisional Application(s) is claimed pursuant to the provisions of **35 U.S.C. §119(e)**:
Application No. **Date Filed**
- ☒ Applicants claim any right to priority from any earlier filed applications to which they may be entitled pursuant to the provisions of **35 U.S.C. §119**, as noted below.

In the matter of the above-identified application for patent, notice is hereby given that the applicants claim as priority:

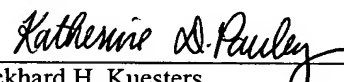
<u>COUNTRY</u>	<u>APPLICATION NUMBER</u>	<u>MONTH/DAY/YEAR</u>
Japan	2001-298533	September 27, 2001

Certified copies of the corresponding Convention Application(s)

- ☐ are submitted herewith
- ☐ will be submitted prior to payment of the Final Fee
- ☒ were filed in prior application Serial No. 09/995,594 filed November 29, 2001
- ☐ were submitted to the International Bureau in PCT Application Number
Receipt of the certified copies by the International Bureau in a timely manner under PCT Rule 17.1(a) has been acknowledged as evidenced by the attached PCT/IB/304.
- ☐ (A) Application Serial No.(s) were filed in prior application Serial No. filed ; and
- ☐ (B) Application Serial No.(s)
☐ are submitted herewith
☐ will be submitted prior to payment of the Final Fee

Respectfully Submitted,

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